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COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Design Documents

1.0 Introduction

Design documents should serve as fully-specified guidelines for implementation of each checkpoint. While **no code should be provided in the documents**, the level of detail should be sufficient to translate directly into verilog. This means that if you were to hand your design to someone, they should be able to build the checkpoint to your specifications without referencing any external resources. During design reviews, **the TAs will thoroughly question anything that is ambiguous or absent in the documents and points will be deducted accordingly**. A good design document should include state machines, block diagrams and timing waveforms.

2.0 State Machines

State machines are generally used to specify the behavior of a system. As such, you will always need them in your design documents. The following are features that should be included in every bubble and arc diagram.

2.1 Functional Labels

State machines should be clearly labeled based on their function within the overall design. If state machines are implemented hierarchically, it is necessary to specify which state in the larger control FSM the subsystem belongs to. States within a given FSM should also be labeled reasonably to make the behavior evident. Additionally, FSMs are typically modules within a larger system and should thus be connected as part of the block diagrams.

2.2 Transitions

All state machines should have labeled transitions regardless of how trivial they may seem. This includes transitions that occur unconditionally on the clock edge or those that occur after a fixed amount of time. Additionally, any input signals whose purpose isn't clear should be specified.

2.3 Outputs

For Moore machines, outputs should be specified at each state using either a truth table or labels on the bubbles themselves. For Mealy machines, outputs should be specified on the arcs using conventional notation.

3.0 Block Diagrams

Block diagrams are used to show the data flow between components and subsystems. A few examples are typically included in the checkpoint specifications, however **block diagrams used in the design documents should be far more detailed than those provided to you.**

3.1 Level of Detail

Block diagrams should be primarily drawn at a systems and component level. This means that designs should contain adders, counters, comparators, shift registers and clustered combinational logic, but need not go any deeper. In some cases, control signals may require individual gates or multiplexers to illustrate data flow.

3.2 Inputs, Outputs and Directional Flow

Blocks included in the block diagram should display all inputs and outputs. Additionally arrowheads should be used to indicate the direction of flow between modules. In some cases it is appropriate to group many signals into a single label to avoid cluttering the diagram, however all signals should be specified elsewhere in the documentation.

3.3 Exploiting Heirarchy

Not all systems are simple enough to fit into a single block diagram. In some cases, subsystems are equally complex and require their own block diagrams. Start with a high level diagram and then specify the block diagrams for each component.

4.0 Timing Waveforms

Timing waveforms are helpful in showing the behavior of your design with respect to time. They are also useful for debugging purposes since they display information in the same way that you would observe it in ChipScope. Whenever a system is extremely sensitive to timing constraints, waveform diagrams are necessary. These need not be exhaustive, however they should show signal behavior for each mode of operation of the system.

5.0 Design Reviews and Grading

As stated earlier, the more that is lacking in the design documents, the more questions you will be asked during design reviews. To avoid being caught off guard, specify everything on paper. Additionally, neatness does matter and anything illegible will be treated as absent. It is strongly advised that you use Visio for your designs, however neatly drawn designs done by hand are also acceptable. Finally, late design documents will not be accepted and they are due within the first 10 minutes of your assigned lab section. If you follow these guidelines, you will not only receive a good grade on the design review, but it will also make your life easier when it comes time to implement the design.